CMS32C030 Datasheet

32-bit microcontrollers based on ARM® Cortex®-M0+

64KB Flash, analog functions, Timers, and communication interfaces.

V0.9.1

Features

- **Operation Environment**
  - Supply voltage range: 2.0V to 5.5V
  - Temperature range: -40℃ to 85℃
  - Low power consumption modes: sleep mode, deep sleep mode
- **Core**
  - ARM® 32-bit Cortex®-M0+ CPU
  - Operation frequency: 48MHz
- **32-Bit Hardware Multiplier**
  - Supports single-cycle 32-bit multiplication operations.
- **Memory**
  - 64KB flash memory with shared program and data storage
  - 1KB dedicated data flash memory
  - 8KB SRAM memory
- **Power and Reset Management**
  - Power-on Reset (POR)
  - Low voltage detection (LVD) (threshold voltage can be set)
- **Clock Management**
  - Internal high-speed oscillator: 48MHz
  - Internal low-speed oscillator: 32KHz
  - XT1 external crystal oscillator: 32.768KHz
- **Enhanced DMA**
  - 3 channels
  - Interrupt trigger start
  - Supports normal mode, repeat mode and chain transfer
- **General-Purpose CRC**
- **GPIO**
  - Up to 30 GPIOs, supports external interrupts
  - All GPIOs support pull-up/pull-down resistor functionality
  - Some GPIOs can be configured for TTL input or Schmitt input
- **High Precision 12-Bit ADC**
  - Conversion rate: 500 Ksps
  - Up to 30 external analog channels
  - Supports single, continuous, scan, and select modes
  - Supports hardware trigger
  - Conversion range: 0 to positive reference voltage
- **Analog Comparators (ACMP0/1)**
  - Multiple selectable positive and negative terminals
  - Supports hysteresis voltage selection: 0mV/20mV
  - Comparator output can be used as a trigger signal for Timer 1
- **Rich Timer Resources**
  - 1x 16-bit advanced control timer (TIM1)
  - 4x 16-bit general-purpose timers (TIM3/TIM14/TIM16/TIM17)
  - 1x windowed watch dog timer (WWDG)
  - 1x independent watch dog timer (IWDG)
  - 1x 15-bit interval timer
  - SysTick timer
- **Rich and Flexible Interfaces**
  - 2-channel general-purpose serial communication unit: Supports 3-wire serial (SSPI), UART, simplified I^2C functions, supports up to 1 UART
  - 1x SPI communication unit: Supports 8-bit and 16-bit transfer frames
  - 1x I^2C interface: Supports standard mode (100 KHz) and fast mode (400 KHz)
  - 1x serial synchronous/asynchronous communication unit (USART): Supports single-wire half-duplex communication
- **Safety Features**
  - Compliant with IEC60730 standards
  - Supports hardware CRC
  - Supports protection of important SFRs to prevent misoperations
  - 128-bit unique ID
- **Serial Two-Wire Debugger (SWD)**

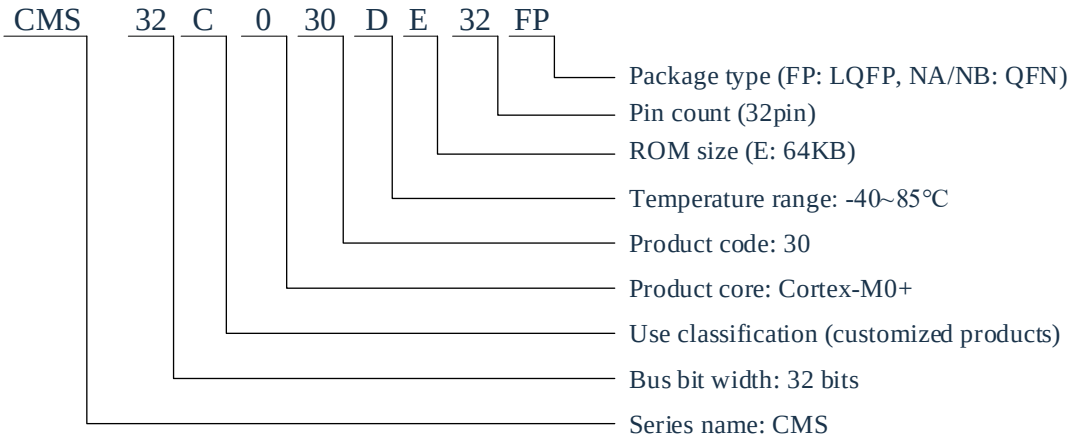
1 Overview

1.1 Brief Introduction

The CMS32C030 uses a high-performance ARM® Cortex®-M0+ 32-bit RISC core, capable of operating at up to 48 MHz. It features high-speed embedded flash memory (8K SRAM, with a maximum of 64KB program/data flash). This product integrates multiple standard interfaces, including I^2C, UART, and SPI. It also includes several timer modules such as advanced timers and general-purpose timers. The system features a 12-bit A/D converter, enabling the acquisition of external sensor signals, which reduces system design costs.

The CMS32C030 also offers excellent low-power performance, supporting both sleep and deep sleep modes, and provides flexible design options.

1.2 Product Model List



Product list of CMS32C030:

Product model	Package	Flash memory	Dedicated data Flash memory	SRAM
CMS32C030DE32FP	32-pin plastic LQFP32 (7x7mm, 0.8mm pitch)	64KB	1KB	8KB
CMS32C030DE32NA	32-pin plastic QFN32 (5x5mm, 0.5mm pitch)			
CMS32C030DE32NB	32-pin plastic QFN32 (4x4mm, 0.4mm pitch)			

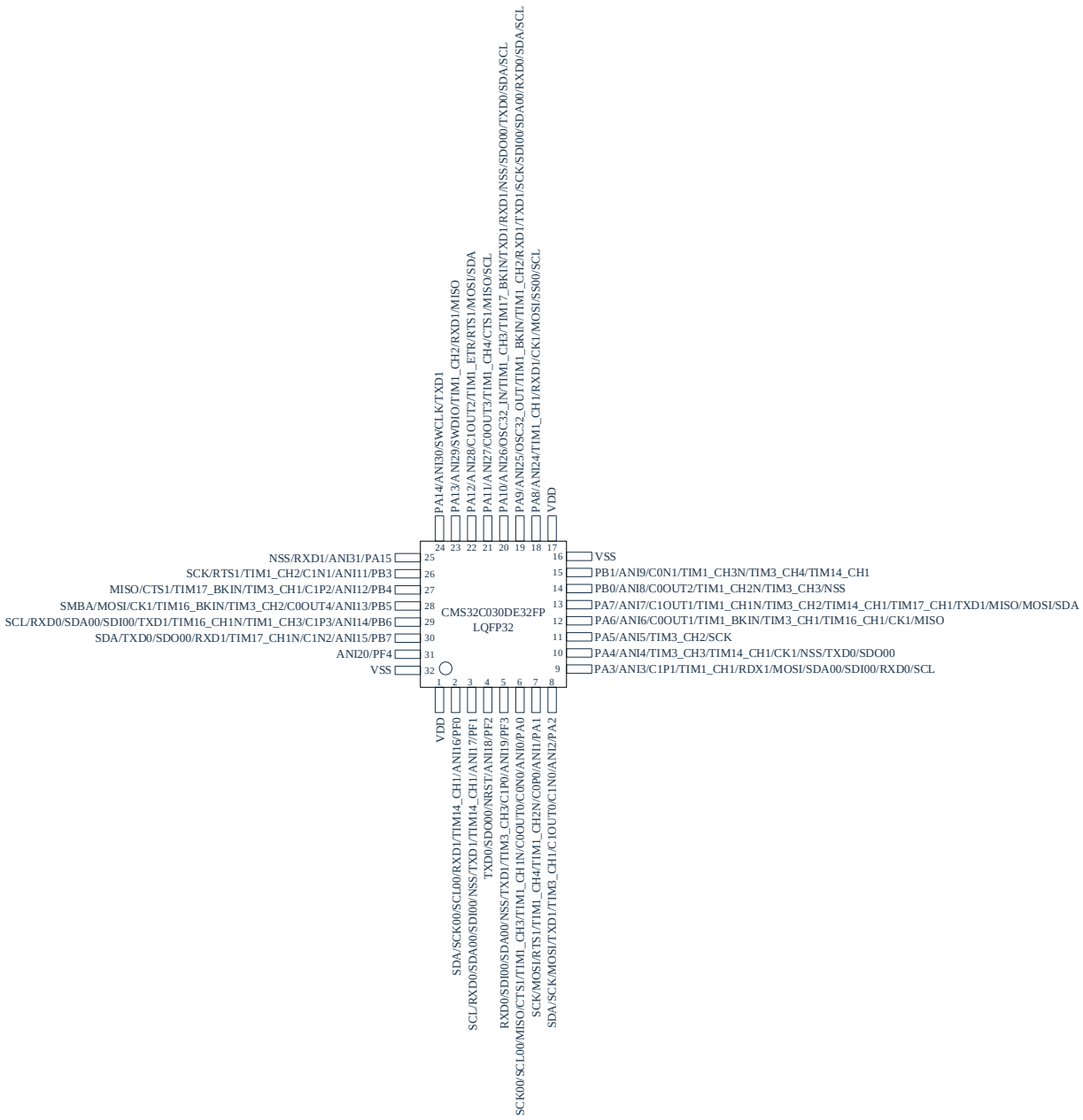
1.3 Product Information

Here is the product information for the CMS32C030 chip:

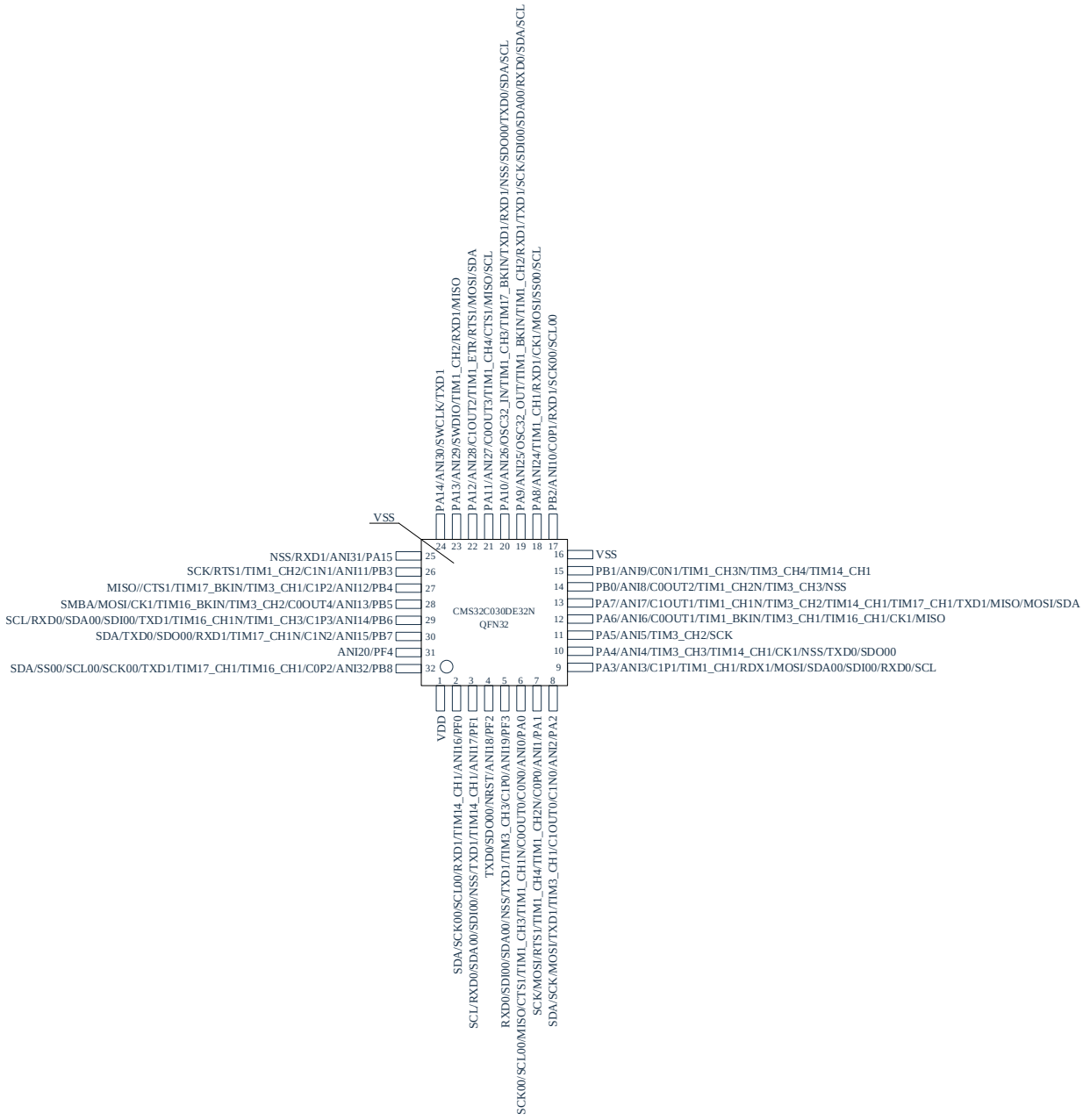
Peripheral interface \ Product model			CMS32C030DE32FP	CMS32C030DE32NA CMS32C030DE32NB
MCU operating voltage			2.0V~5.5V	
Maximum clock frequency			48MHz	
Memory module	ROM		64K	64K
	Data Flash		1K	1K
	SRAM		8K	8K
Timer	SysTick		1	
	WWDG		1	
	IWDG		1	
	16-bit advanced timer		1	
	16-bit universal timer		4	
	15-bit interval timer		1	
Enhanced digital peripheral	CRC		1	
	DMA (3 channels)		1	
Communication module	SAU	SSPI	1	
		UART	1	
		Simplified I^2C	1	
	SPI		1	
	USART		1	
	I^2C		1	
Analog module	12-bit ADC (Number of external channels)		28	30
	ACMP		2	
GPIOS			28	30
LVD			4.0V/3.65V/3.1V/2.95V/2.85V/2.75V/2.65V/2.55V/2.45V/2.0V/1.9V/1.8V	
Operating voltage			2.0V~5.5V	
Operating temperature			-40℃ to 85℃	
Package			LQFP32	QFN32

1.4 Top View

1.4.1 CMS32C030DE32FP

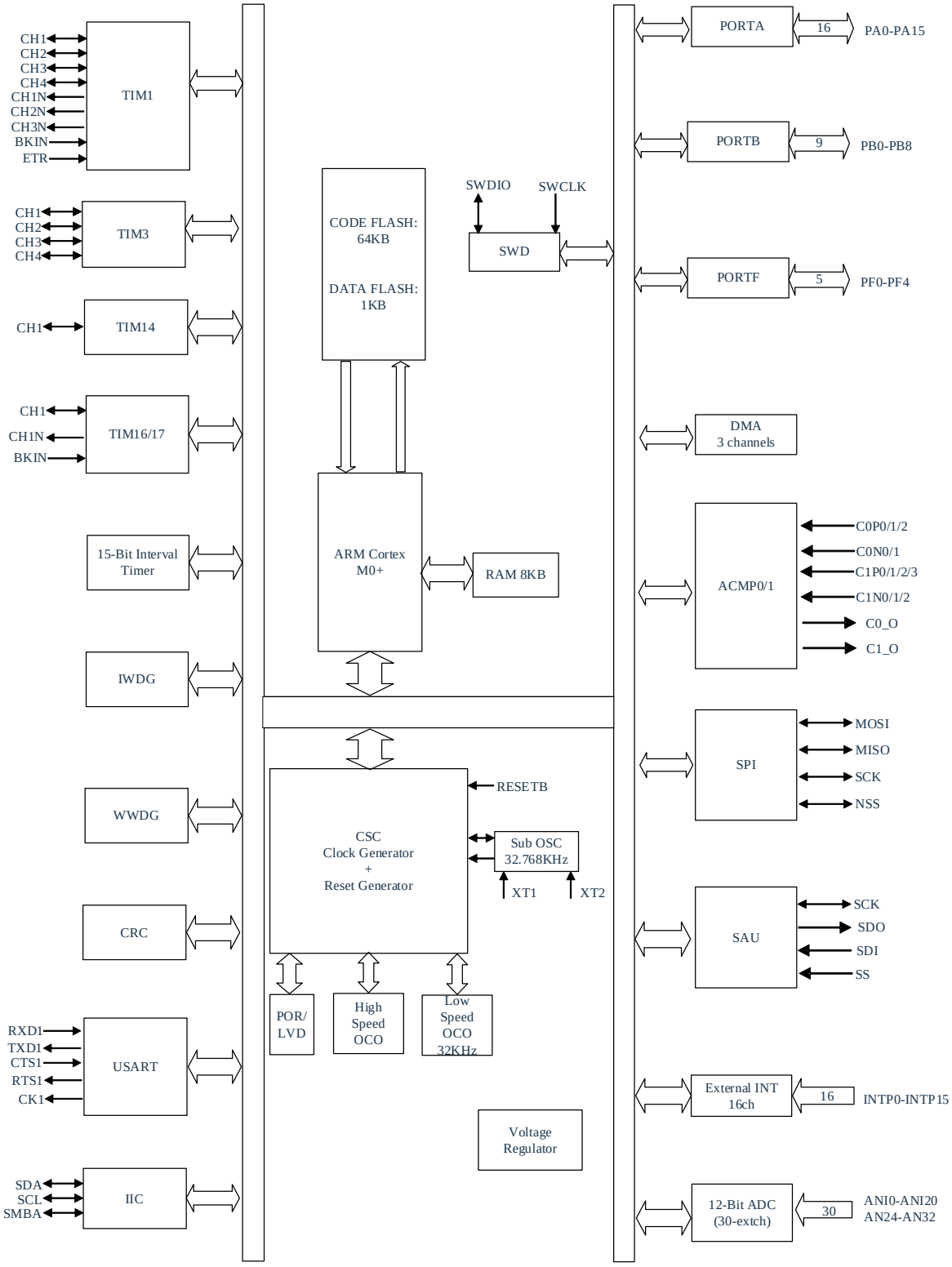


1.4.2 CMS32C030DE32NA/CMS32C030DE32NB

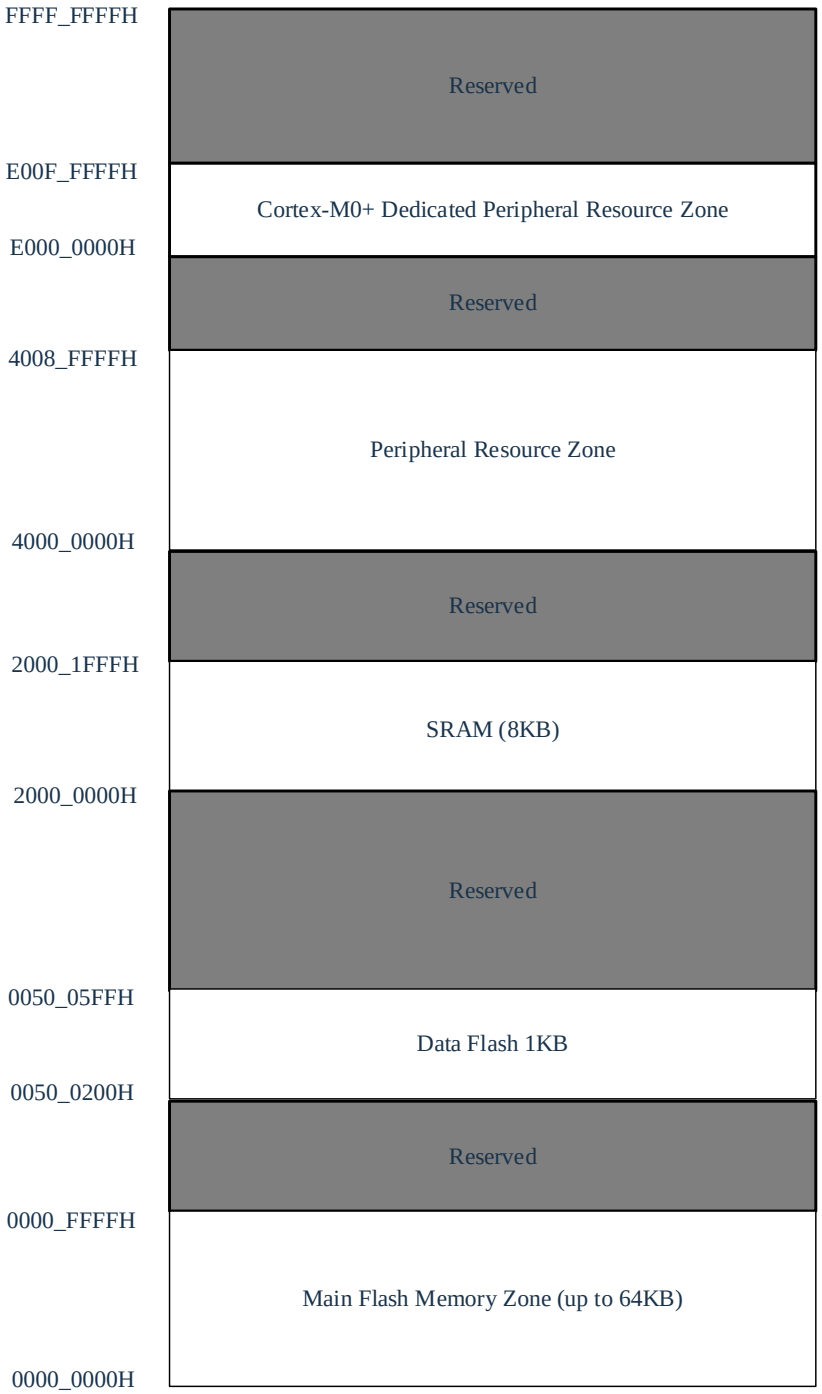


2 Product Block Diagram

2.1.1 CMS32C030DE32NA



3 Memory Map


FFFF_FFFFH
Reserved
E00F_FFFFH
Cortex-M0+ Dedicated Peripheral Resource Zone
E000_0000H
Reserved
4008_FFFFH
Peripheral Resource Zone
4000_0000H
Reserved
2000_1FFFH
SRAM (8KB)
2000_0000H
Reserved
0050_05FFH
Data Flash 1KB
0050_0200H
Reserved
0000_FFFFH
Main Flash Memory Zone (up to 64KB)
0000_0000H

4 Pin Functions

4.1 Port Functions

The symbols in the following table are explained as follows:

Pin type	Symbol description
I/O	Digital input/output
I	Digital input
O	Digital output
AI	Analog input
AO	Analog output
P	Power or ground

Pin number		Pin name	Pin type	Description
LQFP32	QFN32			
6	6	PA0	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI0	AI	ADC channel 0 input
		C0N0	AI	ACMP0 negative input 0
		C0OUT0	O	ACMP0 output channel 0
		CTS1	I	USART hardware flow input
		MISO	I/O	SPI master input/slave output
		SCK00	I/O	Serial interface SSPI00 clock I/O
		SCL00	I/O	Serial interface IIC00 clock I/O
		TIM1_CH1N	O	TIM1 channel 1 complementary output
		TIM1_CH3	I/O	TIM1 channel 3 I/O
7	7	PA1	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI1	AI	ADC channel 1 input
		C0P0	AI	ACMP0 positive input 0
		RTS1	O	USART hardware flow output
		MOSI	I/O	SPI master output/slave input
		SCK	I/O	SPI clock input/output
		TIM1_CH2N	O	TIM1 channel 2 complementary output
		TIM1_CH4	I/O	TIM1 channel 4 input/output
8	8	PA2	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI2	AI	ADC channel 2 input
		C1N0	AI	ACMP1 negative input 0
		C1OUT0	O	ACMP1 output channel 0
		TXD1	O	USART data output
		MOSI	I/O	SPI master output/slave input

Pin number		Pin name	Pin type	Description
LQFP32	QFN32			
		SCK	I/O	SPI clock input/output
		SDA	I/O	IIC data input/output
		TIM3_CH1	I/O	TIM3 channel 1 input/output
9	9	PA3	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI3	AI	ADC channel 3 input
		C1P1	AI	ACMP1 positive input 1
		RXD1	I	USART data input
		MOSI	I/O	SPI master output/slave input
		SDI00	I	Serial interface SSPI00 data input
		SDA00	I/O	Serial interface IIC00 data input/output
		RXD0	I	Serial interface UART0 data input
		SCL	I/O	IIC clock input/output
		TIM1_CH1	O	TIM1 channel 1 input/output
10	10	PA4	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI4	AI	ADC channel 4 input
		CK1	O	USART synchronous mode clock output
		NSS	I/O	SPI slave chip select signal input/output
		SDO00	O	Serial interface SSPI00 data output
		TXD0	O	Serial interface UART0 data output
		TIM3_CH3	I/O	TIM3 channel 3 I/O
		TIM14_CH1	I/O	TIM14 channel 1 input/output
11	11	PA5	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI5	AI	ADC channel 5 input
		SCK	I/O	SPI clock input/output
		TIM3_CH2	I/O	TIM3 channel 2 input/output
12	12	PA6	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI6	AI	ADC channel 6 input
		C0OUT1	O	ACMP0 output channel 1
		CK1	O	USART synchronous mode clock output
		MISO	I/O	SPI master input/slave output
		TIM1_BKIN	I	TIM1 brake signal input
		TIM3_CH1	I/O	TIM3 channel 1 input/output
		TIM16_CH1	I/O	TIM16 channel 1 input/output
13	13	PA7	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI7	AI	ADC channel 7 input
		C1OUT1	O	ACMP1 output channel 1

Pin number		Pin name	Pin type	Description
LQFP32	QFN32			
		TXD1	O	USART data output
		MISO	I/O	SPI master input/slave output
		MOSI	I/O	SPI master output/slave input
		SDA	I/O	IIC data input/output
		TIM1_CH1N	O	TIM1 channel 1 complementary output
		TIM3_CH2	I/O	TIM3 channel 2 input/output
		TIM14_CH1	I/O	TIM14 channel 1 input/output
		TIM17_CH1	I/O	TIM17 channel 1 input/output
18	18	PA8	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI24	AI	ADC channel 24 input
		RXD1	I	USART data input
		CK1	O	USART synchronous mode clock output
		MOSI	I/O	SPI master output/slave input
		SS00	I	Serial interface SSPI00 chip select input
		SCL	I/O	IIC clock input/output
		TIM1_CH1	I/O	TIM1 channel 1 input/output
19	19	PA9	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI25	AI	ADC channel 25 input
		OSC32_OUT	AO	XT1 oscillator output
		RXD1	I	USART data input
		TXD1	O	USART data output
		SCK	I/O	SPI clock input/output
		SDI00	I	Serial interface SSPI00 data input
		SDA00	I/O	Serial interface IIC00 data input/output
		RXD0	I	Serial interface UART0 data input
		SDA	I/O	IIC data input/output
		SCL	I/O	IIC clock input/output
		TIM1_BKIN	I	TIM1 brake input
		TIM1_CH2	I/O	TIM1 channel 2 input/output
20	20	PA10	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI26	AI	ADC channel 26 input
		OSC32_IN	AI	XT1 oscillator input
		RXD1	I	USART data input
		TXD1	O	USART data output
		NSS	I/O	SPI slave chip select signal input/output
		SDO00	O	Serial interface SSPI00 data output
		TXD0	O	Serial interface UART0 data output
		SDA	I/O	IIC data input/output

Pin number		Pin name	Pin type	Description
LQFP32	QFN32			
		SCL	I/O	IIC clock input/output
		TIM1_CH3	I/O	TIM1 channel 3 I/O
		TIM17_BKIN	I	TIM17 brake input
21	21	PA11	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI27	AI	ADC channel 27 input
		C0OUT3	O	ACMP0 output channel 3
		CTS1	I	USART hardware flow input
		MISO	I/O	SPI master input/slave output
		SCL	I/O	IIC clock input/output
		TIM1_CH4	I/O	TIM1 channel 4 input/output
22	22	PA12	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI28	AI	ADC channel 28 input
		C1OUT2	O	ACMP1 output channel 2
		RTS1	O	USART hardware flow output
		MOSI	I/O	SPI master output/slave input
		SDA	I/O	SDA data input/output
		TIM1_ETR	I	TIM1 external trigger signal input
23	23	PA13	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI29	AI	ADC channel 29 input
		SWDIO	I/O	SWD data input/output
		RXD1	I	USART data input
		MISO	I/O	SPI master input/slave output
		TIM1_CH2	I/O	TIM1 channel 2 input/output
24	24	PA14	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI30	AI	ADC channel 30 input
		SWCLK	I	SWD clock input
		TXD1	O	USART data output
25	25	PA15	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI31	AI	ADC channel 31 input
		RXD1	I	USART data input
		NSS	I/O	SPI slave chip select signal input/output
14	14	PB0	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI8	AI	ADC channel 8 input
		C0OUT2	O	ACMP0 output channel 2
		NSS	I/O	SPI slave chip select signal input/output

Pin number		Pin name	Pin type	Description
LQFP32	QFN32			
		TIM1_CH2N	O	TIM1channel 2 complementary output
		TIM3_CH3	I/O	TIM3 channel 3 I/O
15	15	PB1	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI9	AI	ADC channel 9 input
		C0N1	AI	ACMP0 negative input 1
		TIM1_CH3N	O	TIM1 channel 3 complementary output
		TIM3_CH4	I/O	TIM3 channel 4 input/output
		TIM14_CH1	I/O	TIM14 channel 1 input/output
-	17	PB2	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI10	AI	ADC channel 10 input
		C0P1	AI	ACMP0 positive input 1
		RXD1	I	USART data input
		SCK00	I/O	Serial interface SSPI00 clock I/O
		SCL00	I/O	Serial interface IIC00 clock I/O
26	26	PB3	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI11	AI	ADC channel 11 input
		C1N1	AI	ACMP1 negative input 1
		RTS1	O	USART hardware flow output
		SCK	I/O	SPI clock input/output
		TIM1_CH2	I/O	TIM1 channel 2 input/output
27	27	PB4	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI12	AI	ADC channel 12 input
		C1P2	AI	ACMP1 positive input 2
		CTS1	I	USART hardware flow input
		MISO	I/O	SPI master input/slave output
		TIM3_CH1	I/O	TIM3 channel 1 input/output
		TIM17_BKIN	I	TIM17 external brake signal input
28	28	PB5	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI13	AI	ADC channel 13 input
		C0OUT4	O	ACMP0 output channel 4
		CK1	O	USART synchronous mode clock output
		MOSI	I/O	SP1 master output/slave input
		SMBA	I/O	IIC SMBus mode alarm signal input/output
		TIM3_CH2	I/O	TIM3 channel 2 input/output
		TIM16_BKIN	I	TIM16 external brake signal input
29	29	PB6	I/O	GPIO is configured for input, output, pull-up, pull-down, and

Pin number		Pin name	Pin type	Description
LQFP32	QFN32			
				other functions through registers.
		ANI14	AI	ADC channel 14 input
		C1P3	AI	ACMP1 positive input 3
		TXD1	O	USART data output
		SDI00	I	Serial interface SSPI00 data input
		SDA00	I/O	Serial interface IIC00 data input/output
		RXD0	I	Serial interface UART0 data input
		SCL	I/O	IIC clock input/output
		TIM1_CH3	I/O	TIM1 channel 3 I/O
		TIM16_CH1N	O	TIM16 channel 1 complementary output
30	30	PB7	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI15	AI	ADC channel 15 input
		C1N2	AI	ACMP1 negative input 2
		RXD1	I	USART data input
		SDO00	O	Serial interface SSPI00 data output
		TXD0	O	Serial interface UART0 data output
		SDA	I/O	IIC data input/output
		TIM17_CH1N	O	TIM17 channel 1 complementary output
--	32	PB8	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI32	AI	ADC channel 32 input
		C0P2	AI	ACMP0 positive input 2
		TXD1	O	USART data output
		SCK00	I/O	Serial interface SSPI00 clock I/O
		SCL00	I/O	Serial interface IIC00 clock I/O
		SS00	I	Serial interface SSPI00 chip select input
		SDA	I/O	IIC data input/output
		TIM16_CH1	I/O	TIM16 channel 1 input/output
		TIM17_CH1	I/O	TIM17 channel 1 input/output
2	2	PF0	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI16	AI	ADC channel 16 input
		RXD1	I	USART data input
		SCK00	I/O	Serial interface SSPI00 clock I/O
		SCL00	I/O	Serial interface IIC00 clock I/O
		SDA	I/O	IIC data input/output
		TIM14_CH1	I/O	TIM14 channel 1 input/output
3	3	PF1	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI17	AI	ADC channel 17 input

Pin number		Pin name	Pin type	Description
LQFP32	QFN32			
		TXD1	O	USART data output
		NSS	I/O	SPI slave chip select signal input/output
		SDI00	I	Serial interface SSPI00 data input
		SDA00	I/O	Serial interface IIC00 data input/output
		RXD0	I	Serial interface UART0 data input
		SCL	I/O	IIC clock input/output
		TIM14_CH1	I/O	TIM14 channel 1 input/output
4	4	PF2	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI18	AI	ADC channel 18 input
		SDO00	O	Serial interface SSPI00 data output
		TXD0	O	Serial interface UART0 data output
		NRST	I	External reset pin
5	5	PF3	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI19	AI	ADC channel 19 input
		C1P0	AI	ACMP1 positive input 0
		TXD1	O	USART data output
		NSS	I/O	SPI slave chip select signal input/output
		SDI00	I	Serial interface SSPI00 data input
		SDA00	I/O	Serial interface IIC00 data input/output
		RXD0	I	Serial interface UART0 data input
		TIM3_CH3	I/O	TIM3 channel 3 I/O
31	31	PF4	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
		ANI20	AI	ADC channel 20 input
16	16	VSS	P	Ground pin
1	1	VDD	P	Supply voltage input pin
32	-	VSS	P	Ground pin
17	-	VDD	P	Supply voltage input pin

5 Function Summary

5.1 ARM® Cortex®-M0+ Core

The ARM Cortex-M0+ processor is a next-generation product in the ARM processor family, designed specifically for embedded systems. It provides a low-cost platform aimed at meeting the demands of microcontrollers with fewer pins and low power consumption, while offering excellent computational performance and advanced system response to interrupts.

The Cortex-M0+ processor is a 32-bit microcontroller that delivers outstanding code efficiency and high-performance expectations of the ARM core, differentiating it from 8-bit and 16-bit devices with the same memory size. The Cortex-M0+ processor features 32 address lines, supporting memory space up to 4GB.

The CMS32C030 series uses the embedded ARM core, ensuring compatibility with all ARM tools and software.

5.2 Memory

5.2.1 Flash Memory

This product features built-in flash memory that supports programming, erasing, and rewriting with the following functionalities:

- Program and data share 64K of memory space.
- 1KB dedicated data flash memory.
- Supports page erase, with each page size being 512 bytes.
- Supports byte/half-word/word programming.

5.2.2 SRAM

The chip has an embedded SRAM of 8K bytes.

5.3 Clock Generation and Start-Up

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are two types of system clocks and clock oscillation circuits.

5.3.1 Main System Clock

- High-speed on-chip oscillator (High-speed OCO): The frequency can be selected via the option byte for oscillation. After the reset is released, the CPU starts running with this high-speed on-chip oscillator clock by default. The oscillator can be stopped by executing the deep sleep instruction or by setting the HIOSTOP bit. The frequency set by the option byte can be changed using the frequency selection register of the high-speed on-chip oscillator. The maximum frequency is 48 MHz.

5.3.2 Subsystem Clock

- XT1 Oscillator Circuit: By connecting a 32.768 kHz resonator to the pins (XT1 and XT2), a 32.768 kHz clock oscillation can be generated. The oscillation can be stopped by setting the XTSTOP bit.
- Low-speed on-chip oscillator (Low-speed OCO): Generates a clock oscillation at 32 kHz (typical). The low-speed on-chip oscillator clock can be used as the CPU clock. The following peripheral hardware can run using the low-speed on-chip oscillator clock:
  -Independent Watch Dog Timer (IWDG)
  -15-bit interval timer

5.4 Power Management

5.4.1 Power Supply Method

VDD: External power supply, and voltage range is 2.0 to 5.5V.

5.4.2 Power-On Reset

The power-on-reset circuit (POR) has the following functions:

- An internal reset signal is generated when power is applied. If the supply voltage (VDD) is greater than the detection voltage (V_{POR}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- The power supply voltage (VDD) is compared with the detection voltage (V_{POR}) and an internal reset signal is generated when VDD < V_{POR}. However, when the power supply drops, it must be shifted to deep sleep mode or set to reset by voltage detection circuit or external reset before it is less than the operating voltage range. To restart operation, it must be confirmed that the power supply voltage has returned to the operating voltage range.

5.4.3 Voltage Detection

The voltage detection circuit sets the operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) by means of option bytes. The voltage detection (LVD) circuit has the following functions:

- The internal reset or interrupt request signal is generated by comparing the power supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}).
- The detection voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected via the option byte.
- Able to run in deep sleep mode.
- When the power supply rises, the reset state must be maintained by voltage detection circuitry or external reset before the operating voltage range is reached. When the power supply drops, it must be shifted to deep sleep mode or set to reset state by voltage detection circuit or external reset before it is less than the operating voltage range.
- The operating voltage range varies according to the setting of the user option byte.
- The LVD output can be used as a TIM1/TIM16/TIM17 brake input.

5.5 Low-Power Consumption Modes

The product supports two low-power modes to achieve the best trade-off between low power consumption, short startup time, and available wake-up sources:

- Sleep Mode: Entered by executing the sleep instruction. Sleep mode stops the CPU's operating clock while maintaining oscillation of other clocks, such as the high-speed system clock oscillator, high-speed on-chip oscillator, or external low-speed clock oscillator. While this mode doesn't reduce working current as much as deep sleep mode, it is an effective mode when you need to quickly resume processing via interrupt requests or for intermittent operation.
- Deep Sleep Mode: Entered by executing the deep sleep instruction. Deep sleep mode stops the oscillation of both the high-speed system clock oscillator and high-speed on-chip oscillator, effectively halting the entire system. This significantly reduces the chip's operating current. Deep sleep mode can also be interrupted for intermittent operation, but requires a stable waiting period for oscillator stabilization after waking up. If immediate processing is necessary via an interrupt request, sleep mode must be chosen instead.

In both modes, registers, flags, and data memory are preserved with their content set before entering the standby mode. The output latches and output buffers of the input/output ports also retain their state.

5.6 Reset Function

The following eight methods can generate a reset signal:

(1) External reset input through the RESETB pin.
(2) Internal reset generated by the program failure detection of the Windowed Watch Dog Timer (WWDG).
(3) Internal reset generated by the program failure detection of the Independent Watch Dog Timer (IWDG).
(4) Internal reset generated by the Power-On Reset (POR) circuit comparing the power supply voltage with the detection voltage.
(5) Internal reset generated by the Low Voltage Detection (LVD) circuit comparing the power supply voltage with the detection voltage.
(6) Internal reset generated when the System Reset Request register bit (AIRCR.SYSRESETREQ) is set to 1.
(7) Internal reset generated by accessing an invalid memory.
(8) TRIM positive and negative code reset.

Both internal and external resets are the same; after the reset signal is generated, the program execution begins from the user-defined program starting address.

5.7 Interrupt Function

The Cortex-M0+ processor includes a Nested Vectored Interrupt Controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs and 1 Non-Maskable Interrupt (NMI) input. Additionally, the processor supports multiple internal exceptions.

This product handles 23 maskable interrupt requests (IRQ), as detailed in the corresponding chapter of the user manual. The actual number of interrupt sources may vary depending on the product.

5.8 Timers

5.8.1 Advanced Control Timer (TIM1)

The advanced control timer TIM1 contains a 16-bit auto-reload counter, driven by a programmable pre-scaler. This type of timer can be used for various purposes, including measuring the pulse width of input signals (input capture) or generating output waveforms (output compare, PWM, and complementary PWM with dead time insertion).

The advanced timer (TIM1) and general-purpose (TIMx) timers are fully independent and do not share any resources. They can be synchronized.

TIM1 timer has 4 independent channels, which can be used for:

- Input capture
- Output compare
- PWM generation (edge and center-aligned modes)
- Single pulse mode output

TIM1 can reset its output signal to a known state when a brake input is received.

When controlled by external signals, TIM1 can achieve synchronization of multiple interconnected timers.

TIM1 supports incremental (quadrature) encoder and Hall sensor circuits.

TIM1 supports external clock trigger inputs or cycle-by-cycle current management.

TIM1 timer supports DMA functionality.

In MCU debug mode, TIM1 can be set to stop.

5.8.2 General-Purpose Timer (TIM3)

The TIM3 general-purpose timer is a 16-bit auto-reload counter driven by a 16-bit programmable pre-scaler. It has 4 independent channels that can be used for input capture/output compare, PWM, or single pulse mode output.

When controlled by external signals, TIM3 can achieve synchronization of multiple interconnected timers.

TIM3 timer supports DMA functionality.

TIM3 supports incremental (quadrature) encoder and Hall sensor circuits.

TIM3 supports external clock trigger inputs or cycle-by-cycle current management.

In MCU debug mode, TIM3 can be set to stop.

5.8.3 General-Purpose Timer (TIM14)

The TIM14 general-purpose timer is a 16-bit auto-reload counter driven by a 16-bit programmable pre-scaler.

TIM14 has 1 independent channel, which can be used for input capture/output compare, PWM, or single pulse mode output.

In MCU debug mode, TIM14 can be set to stop.

5.8.4 General-Purpose Timer (TIM16/TIM17)

The general timers TIM16/TIM17 are 16-bit auto-reload counters driven by a 16-bit programmable pre-scaler.

TIM16/TIM17 has 1 independent channel, which can be used for input capture/output compare, PWM, or single pulse mode output.

TIM16/TIM17 has complementary outputs with programmable dead-time.

TIM16/TIM17 can reset its output signal to a known state when a brake input is received.

TIM16/TIM17 timers support DMA functionality.

In MCU debug mode, TIM16/17 can be set to stop.

5.8.5 15-Bit Interval Timer

This product has a built-in 15-bit interval timer, which can generate interrupts (INTIT) at a preset time interval, and can be used to wake up from deep sleep mode. The counting clock can be selected from either the external low-speed clock or the on-chip low-speed clock.

5.8.6 Windowed Watch Dog Timer (WWDG)

The windowed watch dog is based on a 7-bit down-counter. When an issue occurs, it can reset the system as a watch dog. The counting clock is the APB prescaled clock. It can generate an early wake-up interrupt. In MCU debug mode, the windowed watch dog can be set to stop.

5.8.7 Independent Watch Dog Timer (IWDG)

The IWDG is best suited for applications that require a watch dog to operate completely independently of the main program and where timing precision is less critical. The IWDG is clocked by a low-speed on-chip oscillator (LSI), so it continues to function even if the main clock fails.

- When the system generates a LOOKUP, the IWDG counter is enabled by force, and after the LOOKUP is revoked, the IWDG counter is disabled.
- The IWDG hardware mode can be enabled through option bytes.
- The IWDG is a wake-up source for deep sleep mode, waking up the system with a reset.
- In MCU debug mode, the independent watch dog can be set to stop.

5.8.8 SysTick Timer

This timer is designed specifically for real-time operating systems, but it can also be used as a standard decrementing counter. Its features include:

- 24-bit down-counter
- Auto-reload capability
- Generates an interrupt (which can be masked) when the counter reaches 0.

5.9 Communication Module

5.9.1 Universal Serial Communication Unit

This product includes 1 Universal Serial Communication Unit with 2 serial channels, capable of supporting 3-wire serial (SSPI), UART, and simplified I^2C communication functions. The functionality of each channel is assigned as follows.

(1) **3-Wire Serial Interface (Simplified SPI)**

Data transmission and reception are synchronized with the serial clock (SCLK) output by the master device.

This is a clock-synchronous communication interface using 3 communication lines: 1 serial clock (SCLK), 1 serial data output (SDO), and 1 serial data input (SDI).

[Data Transmission and Reception]

- 7-bit or 8-bit data length
- Control of the phase for transmitting and receiving data
- MSB/LSB priority selection
- Setting of data level for transmitting and receiving data

[Clock Control]

- Selection of master or slave mode
- Control of the phase for input/output clock
- Transfer cycle generated by the prescaler and internal counter of the channel
- Maximum transfer rate
  Master communication: Max. 6MHz
  Slave communication: Max. 6MHz

[Interrupt Functions]

- Transfer end interrupt, buffer empty interrupt

[Error Detection Flags]

- Overflow error

(2) Simplified SPI with Slave Chip Select Function

Supports SPI serial communication interface with a slave chip select input function. This is a clock-synchronous communication interface using 4 communication lines: 1 slave chip select input (SS), 1 serial clock (SCLK), 1 serial data output (SDO), and 1 serial data input (SDI).

[Data Transmission and Reception]

- 7-bit or 8-bit data length
- Control of the phase for transmitting and receiving data
- MSB/LSB priority selection
- Setting of data level for transmitting and receiving data

[Clock Control]

- Control of the phase for input/output clock
- Transfer cycles generated by the prescaler and internal counter of the channel
- Maximum transfer rate
  Slave communication: Max.6MHz

[Interrupt Functions]

- Transfer end interrupt, buffer empty interrupt

[Error Detection Flags]

- Overflow error

(3) UART

The function of asynchronous communication via 2 lines, Serial Data Transmission (TxD) and Serial Data Reception (RxD). These 2 communication lines transmit and receive data in frames, consisting of a start bit, data, parity bit, and stop bit, using an internal baud rate for asynchronous communication with other devices. Full-duplex UART communication is supported by using two dedicated channels: one for transmission (even channel) and one for reception (odd channel).

[Data Transmission and Reception]

- 7-bit or 8-bit data length
- MSB/LSB priority selection
- Data level setting for transmission and reception, with inversion option
- Parity bit addition and parity function
- Stop bit addition

[Interrupt Functions]

- Transfer end interrupt, buffer empty interrupt
- Error interrupt triggered by frame error, parity error, or overflow error

[Error Detection Flags]

- Frame error, parity error, overflow error

(4) Simplified I²C

This function provides clock-synchronized communication with multiple devices via two lines: Serial Clock (SCL) and Serial Data (SDA). Since this simplified I²C is designed for single-device communication, such as with flash memory or A/D converters, it can only function as the master device. Start and stop conditions must comply with AC characteristics and are handled by software.

[Data Transmission and Reception]

- Master transmission, master reception (only for single-master functionality)
- ACK output and ACK detection features
- 8-bit data length (for address transmission, the high 7 bits specify the address, and the least significant bit is used for R/W control)
- Start and stop conditions generated by software

[Interrupt Functions]

- Transfer end interrupt

[Error Detection Flags]

- ACK error, overflow error

[Unsupported Features in Simplified I²C]

- Slave transmission, slave reception
- Arbitration failure detection
- Wait detection function

5.9.2 Serial Interface IIC

The I²C (Inter-Integrated Circuit) bus interface is used as an interface between the microcontroller and the I²C serial bus. It provides multi-master mode functionality and can control all I²C bus-specific sequences, protocols, arbitration, and timing. It supports both standard and fast modes and is also compatible with SMBus 2.0. It can be used for various purposes, including CRC generation and verification, SMBus (System Management Bus), and PMBus (Power Management Bus). Depending on the device, DMA functionality can be utilized to reduce the workload of the CPU. Its features are as follows:

- Parallel bus/I²C protocol converter
- Multi-master mode functionality: The same interface can be used as both master and slave mode
- I²C master mode features:
  - Clock generation
  - Start and stop bit generation
- I²C slave mode features:
  - Programmable I²C address detection
  - Dual address mode, allowing responses to two slave addresses
  - Stop bit detection
- 7-bit/10-bit addressing and broadcast call generation and detection
- Supports different communication speeds:
  - Standard speed (up to 100 KHz)
  - Fast speed (up to 400 KHz)
- Status flags:
  - Transmit/Receive mode flag
  - Byte transfer end flag
  - I²C busy flag
- Error flags:
  - Arbitration lost in master mode
  - Acknowledgement failure after address/data transfer
  - Detection of erroneous start and stop bits
  - Overflow/underflow after clock stretching is disabled
- Two interrupt vectors:
  - One interrupt triggered by successful address/data byte transfer
  - One interrupt triggered by error status
- Optional clock stretching
- 1-byte buffer with DMA functionality
- Configurable PEC (Packet Error Check) generation or verification:
  - In Tx mode, the PEC value can be transmitted as the last byte
  - PEC error check for the last received byte
- SMBus 2.0 compatibility:
  - 25 ms clock low timeout delay
  - 10 ms cumulative clock low extension for master device

- 25 ms cumulative clock low extension for slave device
- Hardware PEC generation/verification with ACK control
- Supports Address Resolution Protocol (ARP)

- PMBus compatibility

5.9.3 SPI Communication Unit

The Serial Peripheral Interface (SPI) provides half-duplex/full-duplex synchronous serial communication with external devices. The interface can be configured as the master mode, in which case it provides the communication clock (SCK) for the external slave devices. The interface can also operate in a multi-master mode.

It can be used for various purposes, including half-duplex synchronous transfer based on two wires, where one wire can act as a bidirectional data line, or using CRC checks for reliable communication. Its features are as follows:

- Full-duplex synchronous transfer based on three lines
- Half-duplex synchronous transfer based on two wires, where one can act as a bidirectional data line
- 8-bit or 16-bit transfer frame format selection
- Master mode or slave mode operation
- Multi-master mode functionality
- 8 master mode baud rate prescalers (maximum value is $f_{PCLK}/2$)
- Slave mode frequency (maximum value is 6 MHz)
- Faster communication for both master and slave modes
- Hardware or software management of NSS for both master and slave modes: Dynamic switching between master/slave operation
- Programmable clock polarity and phase
- Programmable data order, shift MSB or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- SPI TI mode
- Hardware CRC functionality for ensuring reliable communication:
  - In transmit mode, the CRC value can be sent as the last byte
  - CRC error checking is automatically performed based on the last received byte
- Master mode fault, overflow, and CRC error flags that can trigger interrupts
- 1-byte transmit and receive buffers with DMA functionality: Transmission and reception requests

5.9.4 Serial Synchronous/Asynchronous Communication Unit (USART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) is capable of flexible full-duplex data exchange with external devices, meeting the requirements of industrial standard NRZ asynchronous serial data format for external devices. The USART provides multiple baud rates through a fractional baud rate generator.

It supports synchronous unidirectional communication and half-duplex single-wire communication; it also supports LIN (Local Interconnect Network), IrDA (Infrared Data Association) SIR ENDEC standards, and modem operation (CTS/RTS). Additionally, it supports multiprocessor communication.

High-speed data communication can be achieved by configuring multiple buffers and using DMA. Its features are as follows:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Fractional baud rate generator system
  - Universal programmable baud rate for the transceiver
- Programmable data word length (8 bits or 9 bits)
- Configurable stop bits
  - Supports 1 or 2 stop bits
- LIN master mode synchronization stop symbol transmission and LIN slave mode stop symbol detection
  - When configuring USART for LIN hardware, it can generate a 13-bit stop symbol and detect 10/11-bit stop symbols
- Transmitter clock output for synchronous transmission
- IrDA SIR encoder/decoder
  - In normal mode, supports 3/16-bit duration
- Single-wire half-duplex communication
- Multi-buffer communication configurable using DMA (Direct Memory Access)
  - Use DMA to receive/transmit bytes in reserved SRAM buffers
- Separate enable bits for transmitter and receiver
- Transfer detection flags:
  - Receive buffer is full
  - Transmit buffer is empty
  - Transfer end flag
- Parity check control:
  - Send the parity check bit
  - Check the parity of the received data byte
- Four error detection flags:
  - Overflow error
  - Noise detection
  - Framing error
  - Parity check error
- Ten interrupt sources with flag bits:

  - CTS change
  - LIN stop symbol detection
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Line idle detection
  - Overflow error
  - Framing error
  - Noise error
  - Parity check error
- Multiprocessor communication
  - Enters silent mode if the address does not match
- Wake up from silent mode (via line idle detection or address mark detection)
- Two receiver wake-up modes: address bit (MSB, 9th bit), line idle

5.10 Enhanced DMA

The product has a built-in enhanced DMA controller with 3 DMA channels, enabling data transfer between memory without using the CPU. The features of this module are as follows:

- Supports peripheral interrupt-triggered DMA to perform data transfer.
- Supports normal transfer mode, repeat transfer mode, and chain transfer.

5.11 General-Purpose CRC

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to produce the CRC code from a 32-bit data word. Its features are as follows:

Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7

- $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Single input/output 32-bit data register
- CRC calculation is completed within 4 AHB clock cycles.

5.12 Analog Module

5.12.1 Analog-to-Digital Converter (ADC)

This product includes a 12-bit resolution analog-to-digital converter (ADC), capable of converting analog inputs into digital values. It supports up to 30 ADC input channels (ANI0~ANI20, ANI24~ANI32). The features of this ADC are as follows:

- 12-bit resolution, conversion rate of 500Ksps.
- Trigger modes: Hardware no-wait mode and hardware wait mode.
- Channel selection: Supports single-channel selection and multi-channel scanning modes.
- Conversion modes: Supports one-time conversion and continuous conversion.
- Operating voltage: Supports an operating voltage range of 2.5V ≤ VDD ≤ 5.5V.
- Can detect the built-in reference voltage (0.8V).

The ADC can set various A/D conversion modes through the following mode combinations:

Trigger mode	Software trigger	Start conversion via software operation
	Hardware trigger no-wait mode	Start conversion by detecting hardware trigger.
	Hardware trigger wait mode	In the power-off conversion standby state, the conversion is started by detecting the hardware trigger, and after the A/D power stabilization wait time, the conversion starts automatically.
Channel selection mode	Select mode	Choose one channel for analog input and perform A/D conversion.
	Scan mode	Perform A/D conversion on four analog input channels in sequence. Four continuous channels from ANI0~ANI20 or ANI24~ANI32 can be selected as analog inputs.
Conversion mode	One-time conversion mode	Perform a one-time A/D conversion on the selected channel.
	Continuous conversion mode	Perform continuous A/D conversion on the selected channel until stopped by software.

5.12.2 Analog Comparator (ACMP0/1)

This product includes two internal analog comparators, ACMP0 and ACMP1. The ACMP0/1 features the following:

- Analog input voltage range: (0~VDD)V.
- Supports single-side and dual-side hysteresis.
- Supports hysteresis voltage selection (0mV/20mV - typical value).
- Each comparator’s positive and negative terminals can be multiplexed.
- Output filter time can be selected: 0~512*Tsys.
- Comparator output can trigger Timer 1.
- Output change can generate an interrupt.

5.13 Two-Wire Serial Debugging Port (SW-DP)

The ARM SW-DP interface allows serial debug tools to connect to the microcontroller via a serial line.

5.14 Safety Features

5.14.1 Flash Memory CRC Operation (High-Speed CRC)

The CRC operation detects data errors in the flash memory.

- High-speed CRC: During the initialization process, it can stop the CPU operation and quickly check the entire code flash area.

5.14.2 SFR Guard Function

It prevents the overwriting of important Special Function Registers (SFR) due to CPU failures.

5.14.3 A/D Test Function

It allows self-testing of the A/D converter through the A/D conversion of the positive (+) reference voltage, negative (–) reference voltage, analog input channels (ANI), and the internal reference voltage output.

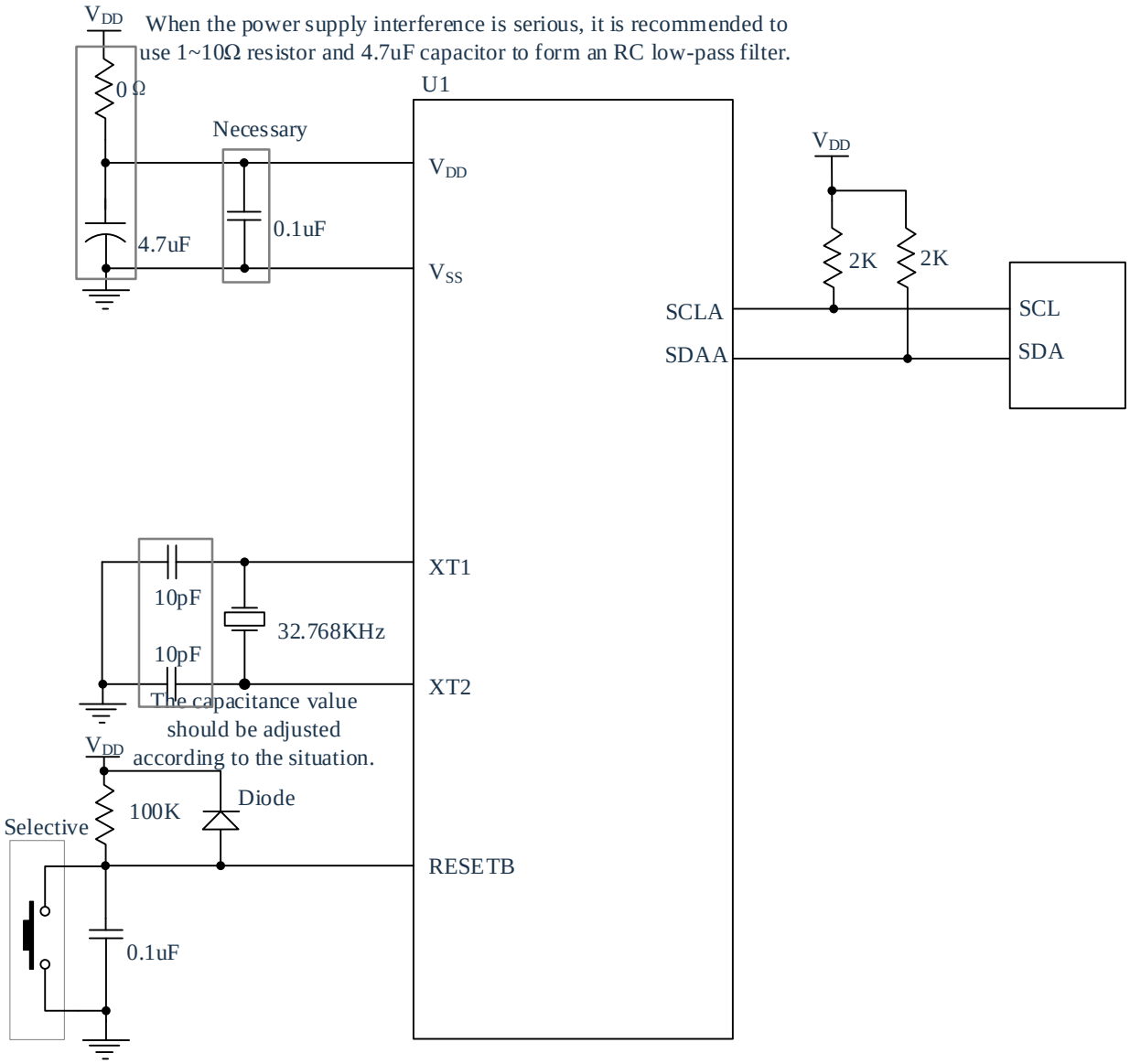
5.14.4 Input/Output Port Digital Output Signal Level Detection Function

When the input/output port is in output mode, it can read the output level of the pin.

6 Electrical Characteristics

6.1 Typical Application Peripheral Circuit

The device connection reference for the peripheral circuit of a typical MCU application is shown as follows.



6.2 Absolute Maximum Voltage Ratings

(T_A= -40~85℃)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5~+6.5	V
Input voltage	V_I	PA0~PA15, PB0~PB8, PF0~PF4	–0.3~VDD+0.3 Note 1	V
Output voltage	V_O	PA0~PA15, PB0~PB8, PF0~PF4	–0.3~VDD+0.3 Note 1	V
Analog input voltage	V_{AI}	ANI0~ANI20, ANI24~ANI31	–0.3~VDD+0.3Note 1	V

Note 1: No more than 6.5V.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks:

1. Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.
2. Use V_{SS} as the reference voltage.

6.3 Absolute Maximum Current Ratings

(T_A= -40~85℃)

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating temperature	-40	+85	℃
T_{ST}	Storage temperature	-65	+150	℃
I_{DD}	Maximum VDD input current	-	150	mA
I_{SS}	Maximum VSS output current	-	150	mA
I_{IO}	Maximum sink current per I/O pin	-	40	mA
	Maximum source current per I/O pin	-	20	mA
	Maximum sink current for all I/O pins	-	150	mA
	Maximum source current for all I/O pins	-	150	mA

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark: Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.

6.4 Oscillation Circuit Characteristics

6.4.1 XT1 Characteristics

(T_A= -40~85℃, 2.0≤VDD≤5.5V, VSS=0V)

Item	Resonator	Condition	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (fxt)	Crystal resonator	2.0V≤VDD≤5.5V	-	32.768	-	kHz

Note 1: This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

Note 2: Please ask the resonator manufacturer to evaluate the circuit after installation, and use it after confirming the oscillation characteristics.

6.4.2 On-Chip Oscillator Characteristics

(T_A= -40~85℃, 2.0≤VDD≤5.5V, VSS=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency (F_{IH}) Note 1,2	-	1.5		48	MHz
High-speed on-chip oscillator clock frequency accuracy	T_A= 25℃	-1		+1	%
	T_A= -20~85℃	-2		+2	%
	T_A= -40~85℃	-4		+4	%
Low-speed on-chip oscillator clock frequency (F_{IL})	-	27.2	32	36.8	kHz

Note 1: The frequency of the high-speed on-chip oscillator is selected via the option byte.

Note 2: This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

Note 3: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.5 DC Characteristics

6.5.1 Pin Characteristics

Symbol	Parameter	Test condition			Min.	Typ.	Max.	Unit
V_{IL1}	Input level, low	Schmitt input			VSS	-	0.3VDD	V
V_{IH1}	Input level, high	Schmitt input			0.7VDD	-	VDD	V
V_{IL2}	Input level, low	PA2/PA3/PF0/PF1	TTL input	4.0V<V_{DD}<5.5V	0		0.8	V
				3V<V_{DD}<4.0V	0		0.5	V
				2.1V<V_{DD}<3V	0		0.32	V
V_{IH2}	Input level, high	PA2/PA3/PF0/PF1	TTL input	4.0V<V_{DD}<5.5V	2.2		VDD	V
				3V<V_{DD}<4.0V	2		VDD	V
				2.1V<V_{DD}<3 V	1.5		VDD	V
V_{OL}	Output voltage, low	VDD=5V, I_{OL}=40mA			-	-	1.5	V
V_{OH}	Output voltage, high	VDD=5V, I_{OH}=20mA			3.5	-	-	V
R_{PH}	Pull-up resistor	-			-	30	-	KΩ
R_{PL}	Pull-down resistor	-			-	30	-	KΩ

6.5.2 Supply Current Characteristics

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	High-speed on-chip oscillator	F_{HOCO}=48MHz, F_{IH}=48MHz Note 3		-	3.5	-	mA
				F_{HOCO} =48MHz, F_{IH} =24MHz Note 3		-	3	-	
			Subsystem clock operation	F_{SUB}=32.768kHz Note 4	Square wave input	-	450	-	uA
					Crystal oscillator connection	-	450	-	
			Low-speed on-chip oscillator	F_{IL}=32kHz Note 8		-	275	-	uA
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	F_{HOCO}=48MHz, F_{IH}=48MHz Note 3		-	2	-	mA
			Subsystem clock operation	F_{SUB}=32.768kHz Note 5	Square wave input	-	350	-	uA
					Crystal oscillator connection	-	350	-	
			Low-speed on-chip oscillator	f_{IL}=32kHz Note 8		-	165	-	uA
	I_{DD3} Note 6	Deep sleep mode Note 7	T_A = -40°C~85°C VDD=5.0V			-	5	-	uA

Note 1: This is the current flowing through VDD, including the input leakage current when the input pins are fixed to either VDD or VSS.

TYP value: The CPU is executing a multiplication instruction (I_{DD1}) and does not include peripheral operating current.

MAX value: The CPU is executing a multiplication instruction (I_{DD1}) and includes peripheral operating current, but does not include current flowing to the A/D converter, LVD circuit, I/O ports, internal pull-up or pull-down resistors, or current during flash memory data rewriting.

Note 2: This is the case where the high-speed on-chip oscillator and the subsystem clock stop oscillating.

Note 3: This is the case where the subsystem clock stops oscillating.

Note 4: This is the case where the high-speed on-chip oscillator stops oscillating.

Note 5: This is the case where the high-speed on-chip oscillator stops oscillating. It does not include the current flowing to the 15-bit interval timer and watch dog timer.

Note 6: Does not include the current flowing to the 15-bit interval timer, and watch dog timer.

Note 7: For the current value when the subsystem clock operates in deep sleep mode, please refer to the current value when the subsystem clock operates in sleep mode.

Note 8: This is the case where the high-speed on-chip oscillator and subsystem clock stop oscillating.

Remarks:

1. F_{HOCO}: High-speed on-chip oscillator clock frequency
   F_{IH}: High-speed on-chip oscillator system clock frequency
2. F_{SUB}: External subsystem clock frequency (XT1/XT2 oscillator frequency)
3. F_{IL}: Low-speed on-chip oscillator clock frequency
4. The typical value temperature condition is T_A = 25°C.

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low speed on-chip oscillator operating current	I_{FIL} Note 1	-		0.5		uA
15-bit interval timer operating current	I_{IT} Note 1,2,3	-		0.02		uA
Watch dog timer operating current	I_{IWDT} Note 1,2,4	F_{IL}=32KHz		0.25		uA
A/D converter operating current	I_{ADC} Note 1,5	ADC @8MHz		0.8		mA
LVD operating current	I_{LVD} Note 1,6	-		0.08		uA

Note 1: This is the current flowing through V_{DD}.

Note 2: This refers to the situation where the high-speed on-chip oscillator stops oscillating.

Note 3: This refers to the current flowing only to the 15-bit interval timer (excluding the current consumed by the low-speed on-chip oscillator and the XT1 oscillator circuit). When the 15-bit interval timer is running in either the run mode or sleep mode, the microcontroller's current value is the sum of I_{DD1} or I_{DD2} and I_{IT}. Additionally, when the low-speed on-chip oscillator is selected, I_{FIL} must be added.

Note 4: This refers to the current flowing only to the watch dog timer (including the current consumed by the low-speed on-chip oscillator). When the watch dog timer is running, the microcontroller's current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT}.

Note 5: This refers to the current flowing only to the A/D converter. When the A/D converter is running in either the run mode or sleep mode, the microcontroller's current value is the sum of I_{DD1} or I_{DD2} and I_{ADC}.

Note 6: This refers to the current flowing only to the Low Voltage Detection (LVD) circuit. When the LVD circuit is running, the microcontroller's current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD}.

Remarks:

1. F_{IL}: Low-speed on-chip oscillator clock frequency
2. The typical value temperature condition is T_A = 25°C.

6.6 AC Characteristics

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (F_{MAIN}) operation	2.0V≤VDD≤5.5V	0.0208	-	0.5	μs
		Subsystem clock (F_{SUB}) operation	2.0V≤VDD≤5.5V	28.5	30.5	31.3	μs
TIM1's CH1~CH4 input high-level width, low-level width	t_{TIH}, t_{TIL}	2.0V≤VDD≤5.5V		1/F_{MCK}+10	-	-	ns
TIM1's CH1~CH4, CH1N~CH3N output frequency	f_{TO}	4.0V≤VDD≤5.5V		-	-	16	MHz
		2.4V≤VDD＜4.0V		-	-	8	MHz
		2.0V≤VDD＜2.4V		-	-	4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 ~ INTP15	2.0V≤VDD≤5.5V	1	-	-	μs
NRST low-level width	t_{RSL}			10	-	-	μs

Remark: F_{CK_CNT}: Timer count clock frequency

6.7 Peripheral Function Characteristics

6.7.1 Universal Interface Unit

(1) UART mode

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	2.0V ≤ VDD ≤ 5.5V	-		F_{MCK}/6	bps
		Theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}		10.6	Mbps

(2) 3-wire SPI mode (master mode, internal clock output)

(T_A= -40~+85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		–40 ~ +85°C		Unit
				Min.	Max.	
SCLKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0V ≤ VDD ≤ 5.5V	31.25	-	ns
			2.7V ≤ VDD ≤ 5.5V	41.67	-	
			2.4V ≤ VDD ≤ 5.5V	65	-	ns
			2.0V ≤ VDD ≤ 5.5V	125	-	ns
SCLKp high/low level width	t_{KH1}, t_{KL1}	4.0V ≤ VDD ≤ 5.5V		T_{KCY1}/2-4	-	ns
		2.7V ≤ VDD ≤ 5.5V		T_{KCY1}/2-5	-	ns
		2.4V ≤ VDD ≤ 5.5V		T_{KCY1}/2-10	-	ns
		2.0V ≤ VDD ≤ 5.5V		T_{KCY1}/2-19	-	ns
SDIp set-up time (for SCLKp↑)	t_{SIK1}	4.0V ≤ VDD ≤ 5.5V		12	-	ns
		2.7V ≤ VDD ≤ 5.5V		17	-	ns
		2.4V ≤ VDD ≤ 5.5V		20	-	ns
		2.0V ≤ VDD ≤ 5.5V		28	-	ns
SDIp hold time (for SCLKp↑)	t_{KSI1}	2.0V ≤ VDD ≤ 5.5V		5	-	ns
Delay time from SCLKp↓→SDOp	t_{KSO1}	2.0V ≤ VDD ≤ 5.5V C=20pF Note 1		-	5	ns

Note 1: C is the load capacitance of the SCLKp and SDOp output lines.

Caution: By using the port input mode register and the port output mode register, select the SDIp pin as the normal input buffer and select the SDOp and SCLKp pins as the normal output mode.

(3) 3-wire SPI mode (slave mode, external clock input)

(T_A= -40~85℃,2.0V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		–40 ~ +85°C		Unit
				Min.	Max.	
SCLKp cycle time	t_{KCY2}	4.0V ≤ VDD ≤ 5.5V	20MHz <f_{MCK}	8/F_{MCK}	-	ns
			f_{MCK} ≤20MHz	6/ F_{MCK}	-	ns
		2.7V ≤ VDD ≤ 5.5V	16MHz <f_{MCK}	8/ F_{MCK}	-	ns
			f_{MCK} ≤16MHz	6/ F_{MCK}	-	ns
		2.4V ≤ VDD ≤ 5.5V		6/ F_{MCK} and ≥500	-	ns
		2.0V ≤ VDD ≤ 5.5V		6/ F_{MCK} and ≥750	-	ns
SCLKp high/low level width	t_{KH2}, t_{KL2}	4.0V ≤ VDD ≤ 5.5V		T_{KCY1}/2-7	-	ns
		2.7V ≤ VDD ≤ 5.5V		T_{KCY1}/2-8	-	ns
		2.0V ≤ VDD ≤ 5.5V		T_{KCY1}/2-18	-	ns
SDIp set-up time (for SCLKp↑)	t_{SIK2}	2.7V ≤ VDD ≤ 5.5V		1/ F_{MCK} +20	-	ns
		2.0V ≤ VDD ≤ 5.5V		1/ F_{MCK} +30	-	ns
SDIp hold time (for SCLKp↑)	t_{KSI2}	2.0V ≤ VDD ≤ 5.5V		1/F_{MCK}+31	-	ns
Delay time from SCLKp↓→SDOp	t_{KSO2}	2.7V ≤ VDD ≤ 5.5V C=30pF Note 1		-	2/ F_{MCK} +44	ns
		2.4V ≤ VDD ≤ 5.5V C=30pF Note 1		-	2/ F_{MCK} +75	ns
		2.0V ≤ VDD ≤ 5.5V C=30pF Note 1		-	2/ F_{MCK} +100	ns

Note 1: C is the load capacitance of the SCLKp and SDOp output lines.

Caution: By using the port input mode register and the port output mode register, select the SDIp pin and the SCLKp pin as normal input buffers, and select the SDOp pin as the normal output mode.

(4) 4-wire SPI mode (slave mode, external clock input)

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		–40 ~ +85°C		Unit
				Min.	Max.	
SSI00 set-up time	t_{SSIK}	DAPmn=0	2.7V ≤ VDD ≤ 5.5V	120	-	ns
			2.0V ≤ VDD ≤ 5.5V	200	-	ns
		DAPmn=1	2.7V ≤ VDD ≤ 5.5V	1/F_{MCK}+120	-	ns
			2.0V ≤ VDD ≤ 5.5V	1/ F_{MCK} +200	-	ns
SSI00 hold time	t_{KSSI}	DAPmn=0	2.7V ≤ VDD ≤ 5.5V	1/ F_{MCK} +120	-	ns
			2.0V ≤ VDD ≤ 5.5V	1/ F_{MCK} +200	-	ns
		DAPmn=1	2.7V ≤ VDD ≤ 5.5V	120	-	ns
			2.0V ≤ VDD ≤ 5.5V	200	-	ns

Caution: By using the port input mode register and the port output mode register, select the SDIp pin and the SCLKp pin as normal input buffers, and select the SDOp pin as the normal output mode.

(5) Simplified IIC mode

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	–40 ~85°C		Unit
			Min.	Max.	
SCLr clock frequency	f_{SCL}	2.7V ≤ VDD ≤ 5.5V Cb= 50 pF, Rb = 2.7 kΩ		1000Note 1	kHz
		2.0V ≤ VDD ≤ 5.5V Cb= 100 pF, Rb = 3 kΩ	-	400Note 1	kHz
		2.0V ≤ VDD ≤ 2.7V Cb= 100 pF, Rb = 5 kΩ	-	300Note 1	kHz
Hold time when SCLr is low	t_{LOW}	2.7V ≤ VDD ≤ 5.5V Cb= 50 pF, Rb = 2.7 kΩ	475	-	ns
		2.0V ≤ VDD ≤ 5.5V Cb= 100 pF, Rb = 3 kΩ	1150	-	ns
		2.0V ≤ VDD ≤ 2.7V Cb= 100 pF, Rb = 5 kΩ	1550	-	ns
Hold time when SCLr is high	t_{HIGH}	2.7V ≤ VDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475	-	ns
		2.0V ≤ VDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150	-	ns
		2.0V ≤ VDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550	-	ns
Data setup time (reception)	$t_{SU:DAT}$	2.7V ≤ VDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	$1/F_{MCK}$+85Note 2	-	ns
		2.0V ≤ VDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	$1/F_{MCK}$ +145Note 2	-	ns
		2.0V ≤ VDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	$1/F_{MCK}$+230 Note 2	-	ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7V ≤ VDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	-	305	ns
		2.0V ≤ VDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	-	355	ns
		2.0V ≤ VDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	-	405	ns

Note 1: It must be set to at least F_{MCK}/4.

Note 2: The setting value of F_{MCK} cannot exceed the hold time for SCLr = “L” and SCLr = “H”.

6.8 Analog Characteristics

6.8.1 A/D Converter Characteristics

Classification of A/D converter characteristics

Input channel \ Reference voltage	Reference voltage (+)=V_{DD} Reference voltage (-)=V_{SS}
ANI0~ANI20, ANI24~ANI31	See the table below
Internal reference voltage	

When selecting reference voltage (+)=VDD, reference voltage (-)=VSS

(T_A= -40~85℃, 2.5V≤V_{DD}≤5.5V, V_{SS}=0V, reference voltage (+)=V_{DD}, reference voltage (-)= V_{SS})

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Overall error Note 1	AINL	12-bit resolution	2.5V≤VDD≤5.5V	-	3	-	LSB
Conversion time Note 3	T_{CONV}	12-bit resolution Conversion target: ANI0~ANI20, ANI24~ANI31	2.5V≤VDD≤5.5V	16			T_{MCLK}
Zero-scale error Note 1	E_{ZS}	12-bit resolution	2.5V≤VDD≤5.5V	-	0	-	LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	2.5V≤VDD≤5.5V	-	0	-	LSB
Integral linearity error Note 1	ILE	12-bit resolution	2.5V≤VDD≤5.5V	-5	-	5	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.5V≤VDD≤5.5V	-2	-	2	LSB
Analog input voltage	V_{AIN}	ANI0~ANI20, ANI24~ANI31		0	-	VDD	V
		Internal reference voltage (2.5V≤VDD≤5.5V)		V_{BGR} Note 2			V

Note 1: Quantization error (±1/2 LSB) is not included.

Note 2: Please refer to “6.8.2 Characteristics of Temperature Sensor/Internal Reference Voltage”.

Note 3: Tmclk refers to the action frequency of the AD, with the maximum action frequency being 8 MHz.

6.8.2 Internal Reference Voltage Characteristics

(T_A= -40~85℃,2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal reference voltage	V_{BGR}	TA=25℃	-	0.8	-	V
Internal reference voltage accuracy	-	TA=25℃	-1	-	+1	%
		TA= -20~85℃	-2.5	-	+2.5	%
		TA= -40~85℃	-4	-	+4	%
Stabilization wait time	t_{AMP}	-	5			μs

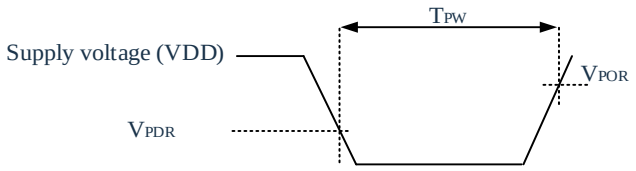
Note 1: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.8.3 POR Characteristics

(T_A= -40~85℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	V_{POR}	When the supply voltage rises	-	1.55	-	V
	V_{PDR}	When the supply voltage drops	-	1.50	-	V
Minimum pulse width Note1	T_{PW}	V_{DD}=V_{PDR}-30mV	300			μs

Note 1: This is the time required for the POR reset when V_{DD} drops below V_{PDR}.



Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8.4 LVD Characteristics

1. Reset mode and interrupt mode

(T_A= -40~85℃, V_{PDR}≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{LVD0}	The power supply voltage is rising.	-	4.05	-	V
		The power supply voltage is falling.	-	4.0	-	V
	V_{LVD1}	The power supply voltage is rising.	-	3.7	-	V
		The power supply voltage is falling.	-	3.65	-	V
	V_{LVD2}	The power supply voltage is rising.	-	3.15	-	V
		The power supply voltage is falling.	-	3.1	-	V
	V_{LVD3}	The power supply voltage is rising.	-	3.0	-	V
		The power supply voltage is falling.	-	2.95	-	V
	V_{LVD4}	The power supply voltage is rising.	-	2.90	-	V
		The power supply voltage is falling.	-	2.85	-	V
	V_{LVD5}	The power supply voltage is rising.	-	2.80	-	V
		The power supply voltage is falling.	-	2.75	-	V
	V_{LVD6}	The power supply voltage is rising.	-	2.70	-	V
		The power supply voltage is falling.	-	2.65	-	V
	V_{LVD7}	The power supply voltage is rising.	-	2.60	-	V
		The power supply voltage is falling.	-	2.55	-	V
	V_{LVD8}	The power supply voltage is rising.	-	2.50	-	V
		The power supply voltage is falling.	-	2.45	-	V
	V_{LVD9}	The power supply voltage is rising.	-	2.05	-	V
		The power supply voltage is falling.	-	2.0	-	V
	V_{LVD10}	The power supply voltage is rising.	-	1.95	-	V
		The power supply voltage is falling.	-	1.9	-	V
	V_{LVD11}	The power supply voltage is rising.	-	1.85	-	V
		The power supply voltage is falling.	-	1.8	-	V
Minimum pulse width	t_{LW}	V_{DD}=V_{LVD}-30mV	300			μs
Detection delay		V_{DD}=V_{LVD}-30mV			300	μs

2. Interrupt & reset mode

(T_A= -40~85°C, V_{PDR} ≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Interrupt & reset mode	V_{LVDA0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Falling reset voltage		-	1.8	-	V
	V_{LVDA1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	1.95	-	V
				Falling interrupt voltage	-	1.90	-	V
	V_{LVDA2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.05	-	V
				Falling interrupt voltage	-	2.0	-	V
	V_{LVDA3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.15	-	V
				Falling interrupt voltage	-	3.1	-	V
	V_{LVDB0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Falling reset voltage		-	2.45	-	-
	V_{LVDB1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.60	-	V
				Falling interrupt voltage	-	2.55	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.70	-	V
				Falling interrupt voltage	-	2.65	-	V
	V_{LVDB3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.70	-	V
				Falling interrupt voltage	-	3.65	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Falling reset voltage		-	2.75	-	-
	V_{LVDD1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.90	-	V
				Falling interrupt voltage	-	2.85	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	3.00	-	V
				Falling interrupt voltage	-	2.95	-	V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	4.05	-	V
				Falling interrupt voltage	-	4.0	-	V

6.8.5 Power Supply Voltage Rise Slope Characteristics

(T_A= -40~85°C, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage rise slope	S_{VDD}				54	V/ms

6.8.6 ACMP0/1 Electrical Parameters

T_A＝25℃, V_{SENSE}＝V_{IN+}-V_{IN-}, V_{DD}＝5V, V_{IN+}=1V, unless otherwise specified.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	2.0	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.3	0.4	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-10.0	-	10.0	mV
V_{CM}	Common mode input voltage range	-40℃~85℃	-0.1	-	V_{DD}-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	50	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	50	-	pA
V_{HYS}	Input hysteresis voltage	V_{DD}=2.0~5.5V, V_{IN+}=0.5V	-	0 ±20	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~85℃	-	-	V_{DD}	V
V_{OL}	Minimum output voltage	-40℃~85℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	80	-	dB
BW	Bandwidth	-	-	150	-	MHz
PSRR	Power supply rejection ratio	V_{DD}=2.0~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	70	-	dB
CMRR	Common mode rejection ratio	V_{DD}=2.0~5.5V, -40℃~85℃	-	90	-	dB
Transient characteristics						
T_{STB}	Stabilization time	-	-	-	2	μs
T_{PGD}	Response delay	V_{DD}=2.5~5.5V, V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.9 Memory Characteristics

6.9.1 Flash Memory

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Symbol	Parameter	Test condition	Min.	Max.	Unit
Tprog	Word write time (32bit)	T_A= –40~85℃		60	μs
Terase	Sector erase time (512B)	T_A= –40~85℃	2	3	ms
	Chip erase time	T_A= –40~85℃	30	40	ms
N_{END}	Number of rewritable times	T_A= –40~85℃	100000		cycle
t_{RET}	Data retention period	T_A = 25℃	25		Years

Note 1: Cycling performed over the whole temperature range.

Note 2: This specification is guaranteed by the design, and is not tested in mass production.

6.9.2 RAM Memory

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, VSS=0V)

Symbol	Parameter	Test condition	Min.	Max.	Unit
Vramhold	RAM hold voltage	T_A= –40~85℃	0.8		V

6.10 EMS Characteristics

6.10.1 ESD Electrical Characteristics

Symbol	Parameter	Test condition	Grade
V_{ESD}	Electrostatic discharge (Human-Body Model HBM)	T_A = + 25℃, ANSI/ESDA/JEDEC JS-001-2024	2
	Electrostatic discharge (Charged-Device Model CDM)	T_A = + 25℃, ANSI/ESDA/JEDEC JS-002-2022	C3

Remark: This specification is guaranteed by the design, and is not tested in mass production.

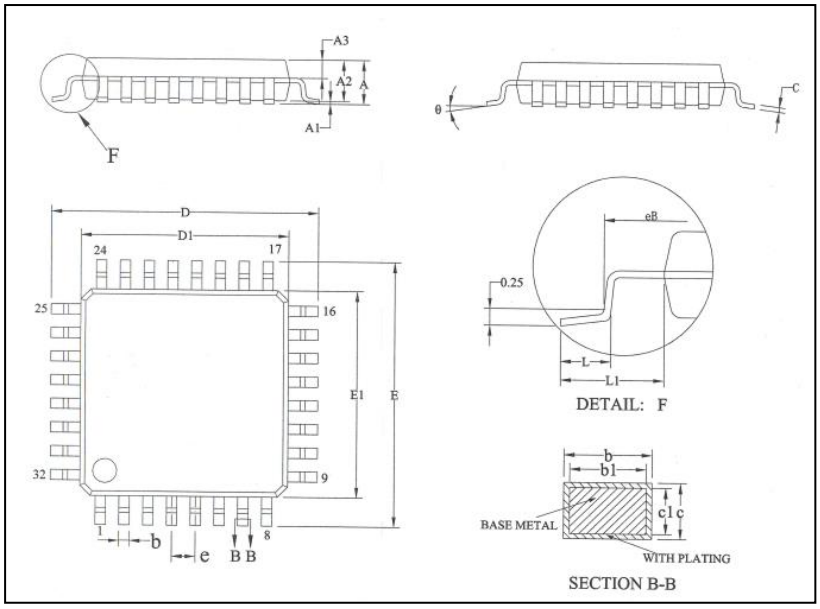
6.10.2 Latch-Up Electrical Characteristics

Symbol	Parameter	Test condition	Level
LU	Static latch-up class	JESD78F	Class I A (T_A = +25°C)

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7 Package Dimensions

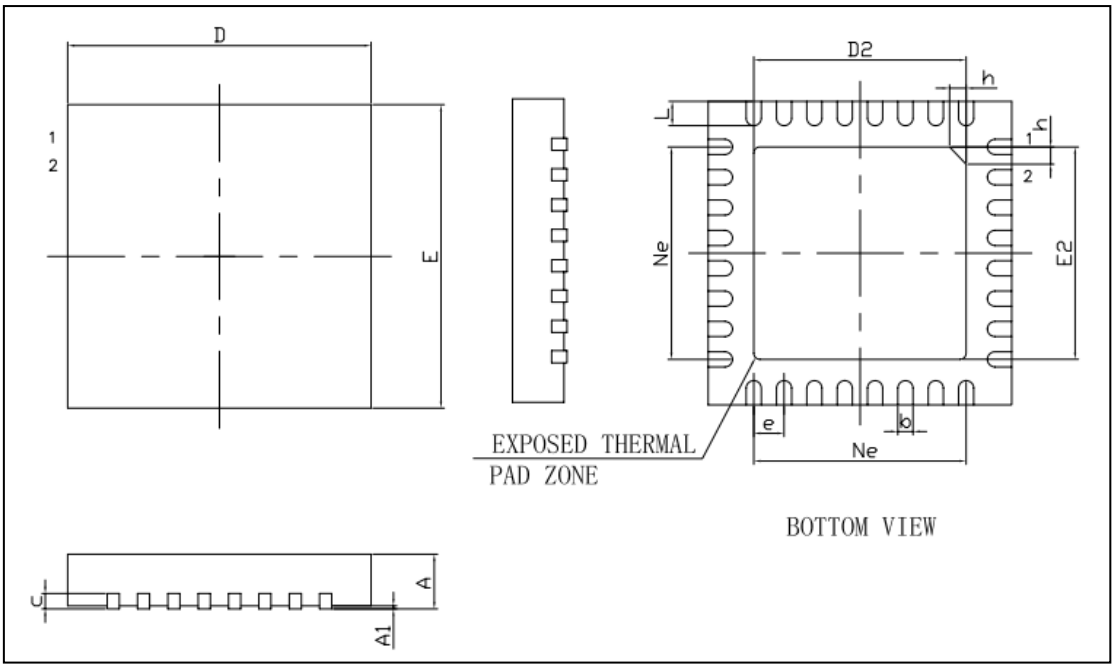
7.1 LQFP32 (7.0x7.0mm, 0.8mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	-	0.43
b1	0.31	-	0.39
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

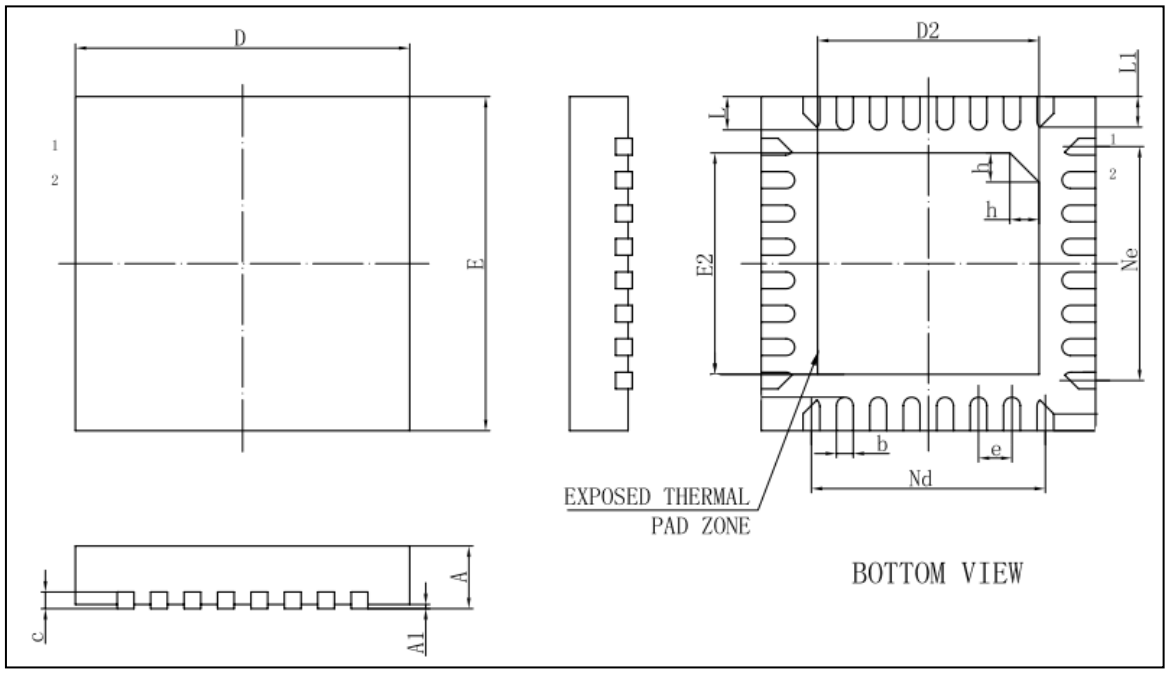
7.2 QFN32 (5.0x5.0mm-0.75, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	-	3.75
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	-	3.75
L	0.30	-	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

7.3 QFN32 (4.0x4.0mm-0.75, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	-	2.80
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	-	2.80
L	0.30	0.40	0.45
L1	0.29	0.35	0.40
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

8 Version History

Version #	Date	Description of changes
V0.0.1	Oct. 2024	Initial release
V0.1.0	Mar. 2025	Format optimization, modification of package size information
V0.1.1	Apr. 2025	Modified Universal Serial Communication Unit, USART-related descriptions
V0.1.2	Apr. 2025	1. Added CMS32C030DE32NB model and package information 2. Modified ADC conversion rate
V0.1.3	May 2025	Removed content related to Clock Output (MCO)
V0.1.4	Jun. 2025	Modified the content of USART, DMA, and electrical parameters
V0.9.0	Jun. 2025	Modified the electrical parameters
V0.9.1	Aug. 2025	1. Modified the Supply voltage range 2. Modified the number of maskable interrupts for the 5.7 interrupt function 3. Modified the ADC conversion rate 4. Update the EMS Characteristics content